IN THE CLAIMS:

1. A method of searching a string of data for a match with a test data string, the method comprising:

receiving an instruction to perform a search operation, the instruction comprising a starting address for the search operation;

routing the instruction to a data string manipulation circuit;

routing the starting address for the search operation from the data string manipulation circuit to a cache memory array;

comparing a test data string with data stored in the cache memory array; and

routing an address of cached data matching the test data string to the data string manipulation circuit.

2. The method of Claim 1, additionally comprising routing the test data string from the data string manipulation circuit to the cache memory array.

3. The method of Claim 2, additionally comprising aligning the test data string with the data stored in the cache memory array prior to said act of comparing.

4. The method of Claim 1, wherein said act of routing an address of cached data is performed by a decoder.

5. The method of Claim 1, wherein the test data string comprises a word.

6. The method of Claim 1, wherein the test data string comprises a doubleword.

7. The method of Claim 1, wherein the test data string comprises a quadword.

8. The method of Claim 1, wherein said act of comparing is performed by a plurality of comparators.

9. The method of Claim 8, wherein the number of the plurality of comparators is equal to the number of bytes in a cache line of the cache memory array.

10. The method of Claim 1, wherein said act of comparing is performed with a plurality of subtractors.

11. The method of Claim 1, wherein said act of comparing is performed in one clock cycle.

12. A method of performing a cache search operation within a digital processing system, the method comprising:

receiving an instruction to perform a search operation, the instruction comprising a starting address and a test data string;

routing the instruction to a data string manipulation circuit;

routing the starting address for the search operation from the data string manipulation circuit to a cache memory;

searching a cache line in the cache memory for data that matches the test data string, wherein said cache line comprises more bytes than the test data string; and

routing an address of cached data matching the test data string to the data string manipulation circuit.

13. The method of Claim 12, additionally comprising aligning the test data string with an offset of the starting address prior to said act of searching.

14. The method of Claim 12, wherein the data string manipulation circuit comprises a bus interface unit.

15. The method of Claim 12, wherein the data string manipulation circuit comprises a memory controller.

16. The method of Claim 12, wherein said act of routing an address of cached data is performed by a decoder.

17. The method of Claim 12, wherein said act of searching the cache line is performed by a plurality of subtractors.

18. The method of Claim 12, wherein said act of searching the cache line is performed by a plurality of comparators.

19. The method of Claim 18, wherein the number of comparators is equal to the number of bytes in the cache line.

20. The method of Claim 12, wherein said act of searching a cache line is performed in a single cycle.

21. The method of Claim 12, wherein said act of routing an address of the matching cached data comprises routing the address of the matching cached data with the lowest address if there are a plurality of matches in the cache line.

22. The method of Claim 12, wherein the test data string comprises a word.

23. A data cache circuit for searching for a data value in a cache memory, the data cache circuit comprising:

a cache data memory comprising a cache line comprising a plurality of bytes of data;

a data source configured to hold a data value, the data value comprising less bytes than the cache line;

an instruction processor configured to search the entire cache line for data matching the data value, the instruction processor comprising:

a first set of inputs coupled to the cache data memory, each of the first set of inputs configured to receive at least one of said plurality of bytes of data of the cache line;

a second set of inputs coupled to the data source and configured to receive at least a portion of the data value from the data source; and

a plurality of outputs; and

a decoder coupled to the outputs of the instruction processor and configured to identify a portion of the cache line that matches at least a portion of the data value.

24. The data cache circuit of Claim 23, wherein the instruction processor comprises a plurality of comparators.

25. The data cache circuit of Claim 24, wherein each comparator is coupled to one input of the first set of inputs, one input of the second set of inputs, and one output of the instruction processor.

26. The data cache circuit of Claim 24, wherein the decoder is configured to identify the matching portions of the cache line when matches from at least two comparators are detected.

27. The data cache circuit of Claim 23, wherein the cache data memory comprises a Level 1 cache.

28. The data cache circuit of Claim 23, wherein the cache data memory comprises a Level 2 cache.

29. The data cache circuit of Claim 23, wherein the data value comprises a plurality of bytes.

30. The data cache circuit of Claim 23, wherein entire the cache line is searched for data matching the data value in one processor cycle.

31. A processor comprising:

a data memory comprising a plurality of cache lines, each cache line comprising a plurality of bytes of data;

an instruction processing circuit configured to receive a test data string and an instruction to perform a search operation, the instruction processing circuit comprising a plurality of inputs coupled to the data memory such that each input is coupled to receive one of the plurality of bytes of data of the cache line, the instruction processing circuit further comprising a plurality of outputs; and

a decoder coupled to the plurality of outputs of the instruction processing circuit and configured to identify a portion of the cache line having data that matches at least a portion of the test data string.

32. The processor of Claim 31, wherein the instruction processing circuit further comprises a plurality of comparators, each comparator configured to compare at least one of the plurality of bytes of data with at least a portion of the test data string.

33. The processor of Claim 32, wherein the number of comparators is equal to the number of bytes in the cache line.

34. The processor of Claim 32, wherein the decoder is configured to identify the matching portions of the cache line when matches from at least two comparators are detected.

35. The processor of Claim 31, wherein the instruction processing circuit comprises a plurality of subtractors.

36. The processor of Claim 31, wherein the test data string comprises a plurality of bytes.

37. The processor of Claim 31, wherein the entire cache line is compared to the test data string in one bus cycle.

38. The processor of Claim 31, wherein the data memory comprises a Level 1 cache.

39. The processor of Claim 31, wherein the instruction processing circuit further comprises a memory controller.

40. A cache memory circuit comprising:

a data source means for holding a data value;

a cache data memory means for holding at least one cache line comprising a plurality of bytes of data; and

a means for searching the cache line, wherein said means for searching is coupled to said cache memory means and said data source means such that the cache line may be searched in one clock cycle for data that matches the data value.

41. The cache memory circuit of Claim 40, further comprising a means for decoding coupled to the means for searching, wherein the means for decoding identifies a portion of the cache line that matches at least a portion of the data value.

42. The cache memory circuit of Claim 40, wherein the means for searching comprises a plurality of subtractors.

43. The cache memory circuit of Claim 40, wherein the means for searching comprises a plurality of comparators.

44. The cache memory circuit of Claim 43, wherein the number of comparators is equal to the number of bytes in the cache line.

45. The cache memory circuit of Claim 40, wherein the data source means comprises an external string execution circuit.

46 The cache memory circuit of Claim 45, wherein the external string execution circuit comprises a bus interface unit.

47. The cache memory circuit of Claim 45, wherein the external string execution circuit is associated with an off-chip memory controller.

48. The cache memory circuit of Claim 43, wherein the means for decoding is configured to identify the matching portions of the cache line when matches from at least two of the comparators are detected.

49. The cache memory circuit of Claim 40, wherein the data value comprises a plurality of bytes.